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CLAIMS:

I claim:

1. A memory device die or chip testing, sorting, and packaging system comprising:

(a) a plurality of test processing units;

(b) a plurality of test connection units;

(c) a plurality of test messaging units;

(d) a plurality of sorting control units;

(e) a plurality of sorting output units;

(f) a plurality of packaging units;

(g) a plurality of packaging control units,

wherein said test processing units perform tests on a plurality of memory devices placed on said test connection units and generate a plurality of memory device type or configuration identifiers, one for each of the memory devices according to test results;

wherein said memory device type or configuration identifiers are forwarded directly or indirectly from said processing units to said test messaging units, said sorting control units, or said packaging control units;

wherein said memory devices are transferred from said test processing units to said sorting output units according to instructions from said sorting control

units based on memory device type or configuration identifiers directly or indirectly from said test messaging units;

wherein said memory devices are packaged into memory chips or memory modules in said packaging units according to instructions from said packaging control units based on memory device type or configuration identifiers directly or indirectly from said test messaging units or said sorting control units.

2. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said test processing units are in-circuit memory test systems, special memory testers, or automatic test equipments.

3. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said test connection units are die probing cards, chip sockets, connectors, adaptors, or printed circuit boards with passive, active, or logic components.

4. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said test messaging units are printing devices, memory devices, storage devices, or electrical, optical, or wireless communication links.

5. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells.

6. The memory device or chip testing, sorting, and packaging system of claim 1,

wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells;

wherein said sorting output units contain a plurality of position selection indicators, each located next to one of the output trays or one of the output entry cells;

wherein said sorting control units accept memory device type or configuration identifiers and light up position selection indicators to identify selected output trays or selected output entry cells to place memory devices.

7. The memory device or chip testing, sorting, and packaging system of claim 1,

wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells;

wherein said sorting control units accept memory device type or configuration identifiers and control a plurality of automatic routing units to transfer memory devices to selected output trays or output entry cells.

8. The memory device or chip testing, sorting, and packaging system of claim 1,

wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells;

wherein said sorting output units contain a plurality of position sensors, each located next to one of the output trays or one of the output entry cells;

wherein said sorting control units monitor the status of position sensors to determine whether memory devices are properly placed in selected output trays or output entry cells.

9. The memory device or chip testing, sorting, and packaging system of claim 1,

wherein said sorting output units contain a plurality of sorted configuration output trays, each having a plurality of output entry cells;

wherein said sorting control units maintain a plurality of memory device configuration mapping tables and determine whether some matching groups of memory devices are to be placed in selected sorted configuration output trays or output entry cells.

10. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said packaging units are wire bonding machines, multiple-chip module assembly machines, or printed circuit board assembly machines.

11. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said packaging control units accept memory device type or configuration identifiers and control said packaging units to perform wire bonding, component placement, or circuit assembly.

12. The memory device or chip testing, sorting, and packaging system of claim 1, further comprises a plurality of detachable memory device carrier units to transport memory devices between test connection units, sorting output units, or packaging units, said device carrier units contain a plurality of device carrier entry cells, a plurality of device descriptions in the form of printed labels or memory storages, and a plurality of interface units to send or receive device descriptions to or from test messaging units, sorting control units, or packaging control units.

13. The memory device or chip testing, sorting, and packaging system of claim 1,

wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells;

wherein said output trays are detachable from the sorting output units.

14. The memory device or chip testing, sorting, and packaging system of claim 1,

wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells;

wherein said output trays contain a plurality of device entry cells, a plurality of device descriptions in the form of printed labels or memory storages, and a plurality of interface units to send or receive device descriptions.

15. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said memory devices are first being sorted and then being packaged.

16. The memory device or chip testing, sorting, and packaging system of claim 1, wherein said memory devices are first being packaged and then being sorted.

17. A memory device die or chip testing and sorting system comprising:

(a) a plurality of test processing units;

(b) a plurality of test connection units;

(c) a plurality of test messaging units;

(d) a plurality of sorting control units;

(e) a plurality of sorting output units;

wherein said test processing units perform tests on a plurality of memory devices placed on said test connection units and generate a plurality of memory device type or configuration identifiers, one for each of said memory devices according to test results;

wherein said memory device type or configuration identifiers are forwarded directly or indirectly from said processing units to said test messaging units, or said sorting control units;

wherein said memory devices are transferred from said test processing units to said sorting output units according to instructions from said sorting control

units based on memory device type or configuration identifiers directly or indirectly from said test messaging units.

18. The memory device or chip testing and sorting system of claim 17, wherein said test processing units are in-circuit memory test systems, special memory testers or automatic test equipments.

19. The memory device or chip testing and sorting system of claim 17, wherein said test connection units are die probing cards, chip sockets, connectors, adaptors, or printed circuit boards with passive, active, or logic components.

20. The memory device or chip testing and sorting system of claim 17, wherein said test messaging units are printing devices, memory devices, storage devices, or electrical, optical, or wireless communication links.

21. The memory device or chip testing and sorting system of claim 17, wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells.

22. The memory device or chip testing and sorting system of claim 17, wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells;

wherein said sorting output units contain a plurality of position selection indicators, each located next to one of the output trays or one of the output entry cells;

wherein said sorting control units accept memory device type or configuration identifiers and light up position selection indicators to identify selected output trays or selected output entry cells to place memory devices.

23. The memory device or chip testing and sorting system of claim 17, wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells;

wherein said sorting control units accept memory device type or configuration identifiers and control a plurality of automatic routing units to transfer memory devices to selected output trays or output entry cells.

24. The memory device or chip testing and sorting system of claim 17, wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells;

wherein said sorting output units contain a plurality of position sensors, each located next to one of the output trays or one of the output entry cells;

wherein said sorting control units monitor the status of position sensors to determine whether memory devices are properly placed in selected output trays or output entry cells.

25. The memory device or chip testing and sorting system of claim 17, wherein said sorting output units contain a plurality of sorted configuration output trays, each having a plurality of output entry cells;

wherein said sorting control units maintain a plurality of memory device configuration mapping tables and determine whether some matching groups of memory devices are to be placed in selected sorted configuration output trays or output entry cells.

26. The memory device or chip testing and sorting system of claim 17, further comprises a plurality of detachable memory device carrier units to transport memory devices between test connection units and sorting output units, said device carrier units contain a plurality of device carrier entry cells, a plurality of device descriptions in the form of printed labels or memory storages, and a plurality of interface units to send or receive device descriptions to or from test messaging units or sorting control units.

27. The memory device or chip testing and sorting system of claim 17, wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells;

wherein said output trays are detachable from the sorting output units.

28. The memory device or chip testing and sorting system of claim 17, wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells;

wherein said output trays contain a plurality of device entry cells, a plurality of device descriptions in the form of printed labels or memory storages, and a plurality of interface units to send or receive device descriptions.

29. A memory device die or chip sorting system comprising:

(a) a plurality of sorting output units;

(b) a plurality of sorting control units;

(c) a plurality of input interface units;

wherein said sorting output units contain a plurality of output trays, each contains a plurality of output entry cells;

wherein said sorting control units accept memory device type or configuration identifiers through said input interface units;

wherein a plurality of memory devices are transferred to said sorting output units according to instructions from said sorting control units based on the memory device type or configuration identifiers.

30. The memory device or chip sorting system of claim 29, wherein said memory device type or configuration identifiers are in the form of printed labels, memory storages, or electrical, optical, or wireless communication signals.

31. The memory device or chip sorting system of claim 29,

wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells;

wherein said sorting output units contain a plurality of position selection indicators, each located next to one of the output trays or one of the output entry cells;

wherein said sorting control units accept memory device type or configuration identifiers and light up position selection indicators to identify selected output trays or selected output entry cells to place memory devices.

32. The memory device or chip sorting system of claim 29,

wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells;

wherein said sorting control units accept memory device type or configuration identifiers and control a plurality of automatic routing units to transfer memory devices to selected output trays or output entry cells.

33. The memory device or chip sorting system of claim 29,

wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells;

wherein said sorting output units contain a plurality of position sensors, each located next to one of the output trays or one of the output entry cells;

wherein said sorting control units monitor the status of position sensors to determine whether memory devices are properly placed in selected output trays or output entry cells.

34. The memory device or chip sorting system of claim 29,

wherein said sorting output units contain a plurality of sorted configuration output trays, each having a plurality of output entry cells;

wherein said sorting control units maintain a plurality of memory device configuration mapping tables and determine whether some matching groups of memory devices are to be placed in selected sorted configuration output trays or output entry cells.

35. The memory device or chip sorting system of claim 29, further comprises a plurality of detachable memory device carrier units to transport memory devices to said sorting output unit, said device carrier units contain a plurality of device carrier entry cells, a plurality of device descriptions in the form of printed labels or memory storages, and a plurality of interface units to send or receive device descriptions.

36. The memory device or chip sorting system of claim 29,

wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells;

wherein said output trays are detachable from the sorting output units.

37. The memory device or chip sorting system of claim 29,

wherein said sorting output units contain a plurality of output trays, each having a plurality of output entry cells;

wherein said output trays contain a plurality of device entry cells, a plurality of device descriptions in the form of printed labels or memory storages, and a plurality of interface units to send or receive device descriptions.